REMARKS

The present Amendment amends claims 2-4, 6 and 8-13, leaves claims 5 and 7 and cancels claim 1. Therefore, the present application has pending claims 2-13.

In the Office Action the Examiner indicated that Figs. 3, 4 and 26 should be designed by a legend "Prior Art"; and objected to the drawings, particularly Fig. 4 as allegedly not complying with the requirements of 37 CFR §1.84(p)(5) because it did not include reference sign "820". Filed on even date herewith is a Proposed Drawing Correction/Replacement Sheet adding the legend "Prior Art" to Figs. 3, 4 and 26. With respect to the reference "820" of Fig. 4, amendments were made to the specification to use the same reference numerals in Fig. 4. Thus, the specification uses only reference numerals illustrated in the drawings. Therefore, the above objections to the drawings are overcome and should be withdrawn.

Claims 1, 9, 12 and 13 stand objected to due to informalities noted by the Examiner in the Office Action. As indicated above, claim 1 was canceled. Therefore, this objection with respect to claim 1 is rendered moot. Amendments were made to the remaining claims 9, 12 and 13 to correct the informalities noted by the Examiner. Therefore, reconsideration and withdrawal of these objections with respect to claim 9, 12 and 13 is respectfully requested.

Claims 1 and 12 stand rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art (Figs. 3, 4 and 26) in view of Yamazaki (U.S. Patent No. 5,600,469); claims 2, 5 and 7 stand rejected under 35 USC §103(a) as being unpatentable over Applicants'

alleged admitted prior art, Yamazaki and further in view of Cloonan (U.S. Patent No. 5,550,815); claims 3 and 6 stand rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and further in view of Aybay (U.S. Patent No. 6,185,522); claim 4 stands rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and further in view of Calvignac (U.S. Patent No. 5,251,206); claim 13 stands rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and further in view of Aybay; claims 8, 10 and 11 stand rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art in view of Cloonan; and claim 9 stands rejected under 35 USC §103(a) as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and further in view of Aybay. As indicated above, claim 1 was canceled. Thus, this rejection with respect to claim 1 is rendered moot. Therefore, reconsideration and withdrawal of the 35 USC §103(a) rejection of claim 1 as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki is respectfully requested.

It should be noted that the cancellation of claim 1 was not intended nor should it be considered as an agreement on Applicants part that the features recited in claim 1 are taught or suggested by any of the references of record. The cancellation of claim 1 was simply intended to expedite prosecution of the present application.

The above noted rejections with respect to the remaining claims 2-13 is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 2-13 are not taught or

suggested by Applicants' alleged admitted prior art, Yamazaki, Cloonan, Aybay and Calvignac whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to the claims to more clearly describe features of the present invention as recited in the claims. Particularly, amendments were made to the claims to recite that the present invention is directed to a packet communication system which supports one-to-many or many-to-one connections between input and output ports so that mixed usage of low speed and high speed line interfaces can be accommodated.

According to the present invention, a packet communication system such as that illustrated in Fig. 1 of the present application is provided. The packet communication system includes a first line interface, a second line interface connectable to a line with a speed lower than that of a line connectable to the first line interface, a crossbar switch and a scheduler that receives packet output requests from the first line interface and the second line interface periodically, and sends packet grants for the crossbar switch accordingly to the first and second line interfaces.

Further, according to the present invention a link capacity between the first line interface and the crossbar switch is larger than a link capacity between the second line interface and the crossbar switch and the number of links forming the link capacity between the first line interface and the crossbar switch is greater than the number of links forming the link capacity between the second line interface and the crossbar switch.

Still further, according to the present invention the scheduler controls the crossbar switch based on the relative link capacities between the first line interface and the crossbar switch and between the second line interface and the crossbar switch.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention now more clearly recited in the claims are not taught or suggested by Applicants' alleged admitted prior art, Yamazaki, Cloonan, Aybay and Calvignac whether taken individually or in combination with each other as suggested by the Examiner.

One of the characteristic features of the present invention as recited in claim 12 is that the scheduler controls the crossbar switch in such a way that the ingress of each one of the first line interfaces is connected to the egress of one of the first line interfaces or an egress of one of the second line interfaces and the ingress of each one of the second line interfaces is connected to up to n egresses of the first line interfaces or the egress of another one of the second line interfaces. By using these features of the present invention regarding the scheduler and crossbar switch, the switching between interfaces of different speeds is achieved.

None of the references of record, particularly Applicants' alleged admitted prior art or Yamazaki teach or suggest the above described features of the present invention as recited in the claims.

Yamazaki discloses a technology wherein data from different speed interfaces are multiplexed in the Multiplexor 4, and are transmitted to the Exchange side, or data from the Exchange side are divided into the bus 6, and are transmitted to each interface (see Fig. 1A of Yamazaki). Thus, Yamazaki does not teach or suggest the features of the present invention regarding switching between different speed interfaces as recited in the claims.

The above described deficiencies of Yamazaki are also evident in Applicants' alleged admitted prior art. In fact, the Examiner readily admits the deficiencies of Applicants' alleged admitted prior art and attempts to supply these deficiencies by combining Applicants' alleged admitted prior art with Yamazaki.

However, as noted above, Yamazaki does not provide the teachings as alleged by the Examiner and in fact is even more deficient of the features of the present invention as now more clearly recited in the claims. Accordingly, combining the teachings of Applicants' alleged admitted prior art and Yamazaki in the manner suggested by the Examiner in the Office Action still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

Thus, both Applicants' alleged admitted prior art and Yamazaki fail to teach or suggest that each of the first line interfaces is connected to the crossbar switch with a link speed V and each of the second line interfaces is connected to the crossbar switch a link speed n x V where n is a number greater than 1 as recited in the claims.

Further, both Applicants' alleged admitted prior art and Yamazaki fail to teach or suggest that the scheduler controls the crossbar switch in such a way that the ingress of each one of the first line interfaces is connected to the egress of one of the first line interfaces or an egress of the one of the second line interfaces and the ingress of each one of the second line interfaces is connected up to n egresses of the first line interfaces or the egress of another one of the second line interfaces as recited in the claims.

Still further, both Applicants' alleged admitted prior art and Yamazaki fail to teach or suggest that the scheduler controls the crossbar switch based on the relative link speeds between each first line interface and the crossbar switch and between each second line interface and the crossbar switch as recited in the claims.

Therefore, since both Applicants' alleged admitted prior art and Yamazaki suffer from the same deficiencies relative to the features of the present invention as recited in the claims, the combination of Applicants' alleged admitted prior art and Yamazaki does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claim 12 as being unpatentable over of Applicants' alleged admitted prior art and Yamazaki is respectfully requested.

One of the characteristic features of the present invention as recited in claims 2, 8, 10 and 11 is that the number of links between the first line interface and the crossbar switch is greater than the number of links between the second line interface and the crossbar switch.

Neither Yamazaki nor Cloonan teach or suggest the above described features of the present invention as recited in the claims. The deficiencies of the teachings of Yamazaki relative to the features of the present invention is described above. Cloonan merely discloses interfaces with the same capacity of transmission. Accordingly, Cloonan naturally doesn't imply interfaces with different line numbers as in the present invention as recited in the claims.

Further, claims 5 and 7 recite other characteristic features of the present invention, particularly regarding the fact that the scheduler receives packet requests of up to the number of links between the first line interface and the crossbar switch from the first line interface, and receives packet requests of up to the number of links between the second line interface and the crossbar switch from the second line interface and the fact that the scheduler sends the first line interface a grant of up to a number of packets equal to the number of links between the first line interface and the crossbar switch, and sends the second line interface a grant of up to a number of packets equal to the number of links between the second line interface and the crossbar switch. Features similar to those recited in claims 2, 5 and 7 can also be found in claims 8, 10 and 11.

The above described features of the present invention now more clearly recited in claims 2, 5, 7, 8, 10 and 11 are not taught or suggested by any of the references of record, particularly Applicants' alleged admitted prior art, Yamazaki and Cloonan.

Thus, each of Applicants' alleged admitted prior art, Yamazaki and Cloonan fails to teach or suggest that the link capacity between the first line and the crossbar switch is larger than a link capacity between the second line

interface and the crossbar switch and the number of links forming the link capacity between the first line interface and the crossbar switch is greater than the number of links forming the link capacity between the second line interface and the crossbar switch as recited in the claims.

Further, each of Applicants' alleged admitted prior art, Yamazaki and Cloonan fails to teach or suggest that the scheduler controls the crossbar switch based on the relative link capacities between the first line interface and the crossbar switch and between the second line interface and the crossbar switch as recited in the claims.

Therefore, since Applicants' alleged admitted prior art, Yamazaki and Cloonan fails to teach or suggest the features of the present invention as now more clearly recited in the claims, combining Applicants' alleged admitted prior art with one or more of Yamazaki and Cloonan does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 2, 5 and 7 as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and Cloonan and the 35 USC §103(a) rejection of claims 8, 10 and 11 as being unpatentable over Applicants' alleged admitted prior art in view of Cloonan is respectfully requested.

Some of the characteristic features of the present invention as recited in claims 3 and 6 are that the scheduler receives more packet output requests from the first line interface than from the second line interface in the same cycle and that the scheduler sends more packet grants to the first line interface than to the second line interface.

Neither Yamazaki nor Aybay teach or suggest the above described features of the present invention as recited in the claims.

Aybay merely discloses scheduling in consideration of QoS, but does not disclose scheduling relative to different speed interfaces as in the present invention. Accordingly, Aybay does not imply the different numbers of received requests and sent grants is related to the differences between the link speeds of the interfaces as in the present invention.

The above described features of the present invention as recited in claims 3 and 6 shown above not to be taught or suggested Applicants' alleged admitted prior art, Yamazaki or Aybay are also evident in claims 9 and 13. Thus, the same arguments presented above with respect to claims 3 and 6 apply as well to claims 9 and 13.

Thus, Applicants' alleged admitted prior art, Yamazaki and Aybay each fails to teach or suggest that the scheduler receives more packet output request from the first line interface than from the second line interface in the same cycle as recited in the claims.

Therefore, since each of Applicants' alleged admitted prior art, Yamazaki and Aybay fails to teach or suggest the features of the present invention as now more clearly recited in the claims, the combination of Applicants' alleged admitted prior art, Yamazaki and Aybay does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 3, 6, 9 and 13 as being unpatentable over Applicants' alleged admitted prior art in view of Yamazaki and Aybay is respectfully requested.

One of the characteristic features of the present invention as recited in claim 4 is that the ratio of the maximum number of packet output requests received by the scheduler from the first line interface to the maximum number of packet output requests received from the second line interface in the same cycle equals the ratio of the number of links between the first line interface and the crossbar switch to the number of links between the second line interface and the crossbar switch.

Neither Yamazaki nor Calvignac teach or suggest the above described features of the present invention as recited in the claims. Calvignac merely discloses changing the data rate dynamically according to the traffic pattern. However, Calvignac does not teach or suggest scheduling relative to the data rate as in the present invention and as such naturally doesn't imply that scheduling is performed relative to the different numbers of received requests and sent grants according to difference of the link speed of the interfaces as in the present invention.

Thus, each of Applicants' alleged admitted prior art, Yamazaki and Calvignac fails to teach or suggest that the ratio of the maximum number of packet output request received by the scheduler from first line interface to the maximum number of packet output request received from the second line interface is in the same cycle equal ratio of the number of links between the first line interface and the crossbar switch to the number of links between the second line interface and the crossbar switch as recited in the claims.

Therefore, since each of Applicants' alleged admitted prior art, Yamazaki and Calvignac fails to teach or suggest the features of the present invention as now more clearly recited in the claims, the combination of

Applicants' alleged admitted prior art, Yamazaki and Calvignac does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claim 4 as being unpatentable over Applicants' alleged admitted prior art, Yamazaki and Calvignac is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-13.

In view of the foregoing amendments and remarks, applicants submit that claims 2-13 are in condition for allowance. Accordingly, early allowance of claims 2-13 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (501.41034X00).

Respectfully submitted,

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